The ETA2001 PWM generator has been designed to provide waveforms for the control of variable speed AC machines, uninterruptible power supplies and other forms of power electronic devices which require pulse width modulation as a means of efficient power control.

The four TTL level PWM outputs (Fig. 2) control the four switches in a single-phase inverter bridge. This is usually via an external isolation and amplification stage.

The ETA2001 is fabricated in CMOS for low power consumption. Information contained within the pulse width modulated sequences controls the shape, power frequency, and amplitude of the output waveform. Parameters such as the carrier frequency, minimum pulse width, and pulse delay time may be defined during the initialization of the device. The pulse delay time (underlap) controls the delay between turning on and off the two power switches in each output leg of the inverter bridge, in order to accommodate variations in the turn-on and turn-off times of families of power devices.

The ETA2001 is easily controlled by a microprocessor or PC and its fully-digital generation of PWM waveforms gives unprecedented accuracy and temperature stability. Precision pulse shaping capability allows optimum efficiency with any power circuitry. The device operates as a stand-alone microprocessor peripheral, reading the power waveform directly from an internal ROM and requiring microprocessor intervention only when operating parameters need to be changed.

A Universal Asynchronous serial Receiver and Transmitter (UART) is used to receive/transmit data from/to the microprocessor/controller.

Rotational frequency is defined to 13 bits for high accuracy and a zero setting is included in order to implement DC injection braking with no software overhead.

Three standard wave shapes are available to cover most applications: pure sinusoid, Triplen and Deadbanded Triplen for reduced switching losses. In addition, any symmetrical wave shape can be integrated on-chip to order.

FEATURES
- Fully Digital Operation
- UART Interfaces
- Power-Frequency Range up to 2kHz
- 13-Bit Speed Control Resolution
- Carrier Frequency Selectable up to 25kHz
- Three Selectable Power Waveforms held in Internal ROM
- Double Edged Regular Sampling
- Selectable Minimum Pulse Width and Underlap Time
- DC Injection Braking

APPLICATIONS
- Single Phase Induction Motor Speed Controllers
- Uninterruptible Power Supplies
- Static Inverter Power Supplies
- Power Waveform Generators

ORDERING INFORMATION
- ETA2001: 24-lead SOIC, industrial temp range.
ET2001

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):
\( V_{CC} = +5V \pm 5\% , T_{AMB} = +25\degree C \)

### DC Characteristics

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Value</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input high voltage</td>
<td>( V_H )</td>
<td>2.7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input low voltage</td>
<td>( V_L )</td>
<td>1.1</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input leakage current</td>
<td>( I_N )</td>
<td>1 μA</td>
<td>V</td>
<td>( I_N = GND ) or ( V_{CC} )</td>
</tr>
<tr>
<td>Output high voltage</td>
<td>( V_{OH} )</td>
<td>4.2</td>
<td>V</td>
<td>( I_{OH} = -20 mA )</td>
</tr>
<tr>
<td>Output low voltage</td>
<td>( V_{OL} )</td>
<td>0.7</td>
<td>V</td>
<td>( I_{OL} = 20 mA )</td>
</tr>
<tr>
<td>Supply current (static)</td>
<td>( I_{CC} \text{ (static)} )</td>
<td>5.5 V</td>
<td>mA</td>
<td>Idle 16 MHz</td>
</tr>
<tr>
<td>Supply current (dynamic)</td>
<td>( I_{CC} \text{ (dynamic)} )</td>
<td>14 V</td>
<td>mA</td>
<td>Active 16 MHz</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>( V_{CC} )</td>
<td>4.5 V</td>
<td>5.0 V</td>
<td>5.5 V</td>
</tr>
</tbody>
</table>

### AC Characteristics

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Value</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock frequency</td>
<td>( I_{CLK} )</td>
<td>8</td>
<td>16</td>
<td>MHz</td>
</tr>
<tr>
<td>Clock duty cycle</td>
<td>( D_{CLK} )</td>
<td>40</td>
<td>60</td>
<td>%</td>
</tr>
<tr>
<td>SET TRIP = 1 ( \rightarrow ) outputs tripped</td>
<td>( t_{TRIP} )</td>
<td>0.25</td>
<td>25</td>
<td>μS</td>
</tr>
<tr>
<td>SET TRIP = 0 ( \rightarrow ) outputs tripped</td>
<td>( t_{TRIP} )</td>
<td>0.25</td>
<td>25</td>
<td>μS</td>
</tr>
</tbody>
</table>

### ABSOLUTE MAXIMUM RATINGS

Supply voltage, \( V_{CC} \)................. ................................. 6.0V
Voltage on any pin......................... ................................. -1.0V to \( V_{CC} \)+0.5V
Current through any I/O pin................. ................................. 20.0 mA
Storage temperature......................... ................................. -65°C to +150°C
Operating temperature range................. ................................. -40°C to +105°C

Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

### PIN DESCRIPTIONS

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Name</th>
<th>Type</th>
<th>Function</th>
<th>Pin No.</th>
<th>Name</th>
<th>Type</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>LT</td>
<td>O</td>
<td>Left-side, Top power switch</td>
<td>24</td>
<td>LB</td>
<td>O</td>
<td>Left-side, Bottom power switch</td>
</tr>
<tr>
<td>2</td>
<td>ZPP</td>
<td>O</td>
<td>Zero Phase Pulse</td>
<td>23</td>
<td>NC</td>
<td>-</td>
<td>Not Connect</td>
</tr>
<tr>
<td>3</td>
<td>TRIP</td>
<td>O</td>
<td>Output trip status; active low</td>
<td>22</td>
<td>NC</td>
<td>-</td>
<td>Not Connect</td>
</tr>
<tr>
<td>4</td>
<td>SET TRIP</td>
<td>I</td>
<td>Set output trip</td>
<td>21</td>
<td>NC</td>
<td>-</td>
<td>Not Connect</td>
</tr>
<tr>
<td>5</td>
<td>TXD</td>
<td>O</td>
<td>UART TX</td>
<td>20</td>
<td>NC</td>
<td>-</td>
<td>Not Connect</td>
</tr>
<tr>
<td>6</td>
<td>VCC</td>
<td>P</td>
<td>Positive power supply</td>
<td>19</td>
<td>DCAP</td>
<td>P</td>
<td>Decoupling CAPacitor</td>
</tr>
<tr>
<td>7</td>
<td>GND</td>
<td>P</td>
<td>Negative power supply (0V)</td>
<td>18</td>
<td>GND</td>
<td>P</td>
<td>Negative power supply (0V)</td>
</tr>
<tr>
<td>8</td>
<td>RT</td>
<td>O</td>
<td>Right-side, Top power switch</td>
<td>17</td>
<td>VCC</td>
<td>P</td>
<td>Positive power supply</td>
</tr>
<tr>
<td>9</td>
<td>RB</td>
<td>O</td>
<td>Right-side, Bottom power switch</td>
<td>16</td>
<td>NC</td>
<td>-</td>
<td>Not Connect</td>
</tr>
<tr>
<td>10</td>
<td>XTL1</td>
<td>I</td>
<td>XTL Input</td>
<td>15</td>
<td>RST</td>
<td>I</td>
<td>Reset internal counters, active low</td>
</tr>
<tr>
<td>11</td>
<td>XTL2</td>
<td>O</td>
<td>XTL Output</td>
<td>14</td>
<td>NC</td>
<td>-</td>
<td>Not Connect</td>
</tr>
<tr>
<td>12</td>
<td>RXD</td>
<td>I</td>
<td>UART RX</td>
<td>13</td>
<td>NC</td>
<td>-</td>
<td>Not Connect</td>
</tr>
</tbody>
</table>
FUNCTIONAL DESCRIPTION
An asynchronous method of PWM generation is used with uniform or ‘double-edged’ regular sampling of the waveform stored in the internal ROM as illustrated in Fig. 3.

The triangle carrier wave frequency is selectable up to 25kHz, enabling ultrasonic operation for noise critical applications. Power frequency ranges of up to 2kHz are possible, with the actual output frequency resolved to 13-bit accuracy within the chosen range in order to give precise motor speed control and smooth frequency changing.

PWM output pulses can be ‘tailored’ to the inverter characteristics by defining the minimum allowable pulse width (the ETA2001 will delete all shorter pulses from the ‘pure’ PWM pulse train) and the pulse delay (underlap) time, without the need for external circuitry. This gives cost advantages in both component savings and in allowing the same PWM circuitry to be used for control of a number of different motor drive circuits simply by changing the microprocessor software.

Power frequency amplitude control is also provided with an overmodulation option to assist in rapid motor braking. Alternatively, braking may be implemented by setting the rotational speed to 0Hz. This is termed ‘DC injection braking’, in which the rotation of the motor is opposed by allowing DC to flow in the windings.

A trip input allows the PWM outputs to be shut down immediately, overriding the microprocessor control in the event of an emergency. Other possible ETA2001 applications are as a 1-phase waveform generator as part of a switched-mode power supply (SMPS) or of an uninterruptible power supply (UPS). In such applications the high carrier frequency allows a very small switching transformer to be used.

MICROPROCESSOR INTERFACE
The ETA2001 interfaces to the controlling microprocessor by means of a standard UART.

Byte Format
Baud Rate: The baud rate can be set to one of follows: 9600, 14400, 19200, 28800, 38400, 57600 and 76800, the device is always set to 9600 baud rate when power on.
Serial Bit Format: 1 Start Bit
8 Data Bits
1 Stop Bit
+--------------------------------------------------
10 Bits Total

Block Format
A Communication Block is defined as a Command byte, optional data bytes, and a CHK byte. A block is limited to a maximum of sixteen (16) bytes.

CHK Byte: A CHK byte must be sent at the end of each block of data. The CHK byte is a checksum calculated by adding the Command byte and all DATA bytes. The CHK byte is not included in the summation. The carry bit for CHK additions is ignored since the CHK byte is limited to eight bits.

The following example shows a CHK byte calculation for a CTRL_WR command sent to the device. See COMMUNICATION COMMAND DESCRIPTION for details of byte meanings.
05H WRITE Control Register
B8H R0
27H R1
FFH R2
+------------------------------------------------------------------
1E3H Therefore the CHK byte would be equal to E3H
A checksum will be performed on all full blocks of communication.
CONTROLLING THE ETA2001

The ETA2001 is controlled by loading data into a 40-bit initialization register and a 24-bit control register via the UART interface.

The initialization register would normally be loaded before motor operation (i.e., prior to the PWM outputs being activated) and sets up the basic operating parameters associated with the motor and inverter. This data would not normally be updated during motor operation. The control register is used to control the PWM outputs (and hence the motor) during operation e.g., stop/start, speed, amplitude etc. and would normally be loaded and changed only after the initialization register has been loaded.

Initialization Register Function

The 40-bit initialization register contains parameters which, under normal operation, will be defined during the power-up sequence. These parameters are particular to the drive circuitry and therefore changing these parameters during a PWM cycle is not recommended. Information in this register should only be modified while RST is active (i.e. low) so that the PWM outputs are inhibited (low) during the updating process.

The parameters set in the initialization register are as follows:

Carrier frequency

Low carrier frequencies reduce switching losses where as high carrier frequencies increase waveform resolution and can allow ultrasonic operation.

Power frequency range

This sets the maximum power frequency that can be carried within the PWM output waveforms. This would normally be set to a value to prevent the motor system being operated outside its design parameters.

Pulse delay time (‘underlap’)

For each phase of the PWM cycle there are two control signals, one for the top switch connected to the positive inverter DC supply and one for the bottom switch connected to the negative inverter DC supply. In theory, the states of these two switches are always complementary. However, due to the finite and non-equal turn-on and turn-off times of power devices, it is desirable when changing the state of the output pair, to provide a short delay time during which both outputs are off in order to avoid a short circuit through the switching elements.

Pulse deletion time

A pure PWM sequence produces pulses which can vary in width between 0% and 100% of the duty cycle. Therefore, in theory, pulse widths can become infinitesimally narrow. In practice this causes problems in the power switches due to storage effects and therefore a minimum pulse width time is required. All pulses shorter than the minimum specified are deleted.

Waveform

Three power waveforms are included as standard with the ETA2001: Sinusoid, Triplen and Deadbanded Triplen.

Initialization Register Programming

The initialization register data is loaded in 8-bit segments into the five 8-bit temporary registers R0-R4. When all the initialization data has been loaded into these registers it is transferred into the 40-bit initialization register.

Carrier frequency selection

The carrier frequency is selected as a proportion of the preconcerted frequency by the 13-bit carrier frequency select word, CFS.

The carrier frequency, $f_{\text{CARR}}$, is then given by:

$$f_{\text{CARR}} = \frac{1 \times 10^5 \times \text{cfs}}{2048}$$

where $25 \leq \text{cfs} \leq 5120$. If cfs selected out of the range, it will be limited to the boundary.
Power frequency range selection

The power frequency range selected here defines the maximum limit of the power frequency. The operating power frequency is controlled by the 13-bit Power Frequency Select (PFS) word in the control register but may not exceed the value set here.

The power frequency range is a function of the carrier waveform frequency \( f_{\text{CARR}} \) and a multiplication factor \( m \), determined by the 3-bit FRS word. The value of \( m \) is determined as shown in Table 1.

<table>
<thead>
<tr>
<th>FRS word</th>
<th>101</th>
<th>100</th>
<th>011</th>
<th>010</th>
<th>001</th>
<th>000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value of ( m )</td>
<td>32</td>
<td>16</td>
<td>8</td>
<td>4</td>
<td>2</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 1 Values of carrier frequency multiplication factor \( m \)

The power frequency range, \( f_{\text{RANGE}} \), is then given by:

\[
f_{\text{RANGE}} = \frac{f_{\text{CARR}}}{384} \times m
\]

where \( f_{\text{CARR}} \) = carrier frequency and \( m = 1, 2, 4, 8, 16 \) or 32 (as set by FRS).

Pulse delay time

The pulse delay time affects all four PWM outputs by delaying the rising edges of each of the outputs by an equal amount.

The pulse delay time is a function of the carrier waveform frequency and \( pdy \), defined by the 8-bit pulse delay time select word (PDY).

The pulse delay time, \( t_{\text{pd}} \), is then given by:

\[
t_{\text{pd}} = \frac{pdy}{f_{\text{CARR}} \times 2048}
\]

where \( pdy = 0 - 255 \) (as set by PDY) and \( f_{\text{CARR}} \) = carrier frequency.

Pulse deletion time

To eliminate short pulses the true PWM pulse train is passed through a pulse deletion circuit. The pulse deletion circuit compares pulse widths with the pulse deletion time set in the initialization register. If a pulse (either positive or negative) is greater than or equal in duration to the pulse deletion time, it is passed through unaltered, otherwise the pulse is deleted.

The pulse deletion time, \( t_{\text{pd}} \), is a function of the carrier waveform frequency and \( pdt \), defined by the 8-bit pulse deletion time word (PDT).

The pulse deletion time, \( t_{\text{pd}} \), is then given by:

\[
t_{\text{pd}} = \frac{pdt}{f_{\text{CARR}} \times 2048}
\]

where \( pdt = 0 - 255 \) (as set by PDT) and \( f_{\text{CARR}} \) = carrier frequency.

Waveform Selection

Three waveform are included as standard with the ETA2001. A pure sine wave is available for applications where waveform purity is important such as static inverter power supplies, uninterruptable power supplies and for driving single or to phase induction motors.

For single phase induction motor control a Triplen waveform is included which provides maximum utilization of the inverter DC link voltage using a harmonic injection technique. Also for motor control, a Deadbanded Triplen waveform may be selected which in addition to providing DC link voltage boost, acts to reduce the number of switching events in the power semiconductors in order to reduce the switching losses. Asymmetrical technique is used to ensure that each power semiconductor benefits to the degree.

Control Register Function

This 24-bit register contains the parameters that would normally be modified during PWM cycles in order to control the operation of the motor.

The parameters set in the control register are as follows:

- **Power frequency (speed)**
  - Allows the power frequency of the PWM outputs to be adjusted within the range specified in the initialization register.

- **Power frequency amplitude**
  - By altering the widths of the PWM output pulses while maintaining their relative widths, the amplitude of the power waveform is effectively altered whilst maintaining the same power frequency.

- **Overmodulation**
  - Allows the output waveform amplitude to be doubled so that a quasi-square wave is produced. A combination of overmodulation and a lower power frequency can be used to achieve rapid braking in AC motors.

- **Output inhibit**
  - Allows the outputs to be set to the low state while the PWM generation continues internally. Useful for temporarily inhibiting the outputs without having to to change other register contents.

Control Register Programming

The control register should only be programmed once the initialization register contains the basic operating parameters of the ETA2001.

As with the initialization register, control register data is loaded into the three 8-bit temporary registers \( R0 \) - \( R2 \). When all the data has been loaded into these registers it is transferred into the 24-bit control register.
### ETA2001

<table>
<thead>
<tr>
<th>OM</th>
<th>INH</th>
<th>PFS12</th>
<th>PFS11</th>
<th>PFS7</th>
<th>PFS9</th>
<th>PFS8</th>
</tr>
</thead>
<tbody>
<tr>
<td>\times \quad 0</td>
<td>= \quad \text{DISABLED}</td>
<td>1</td>
<td>= \quad \text{ACTIVE}</td>
<td>\text{RESERVED}</td>
<td>\text{OUTPUT}</td>
<td>\text{INHIBIT BIT}</td>
</tr>
</tbody>
</table>

#### Power frequency selection
The power frequency is selected as a proportion of the power frequency range (defined in the initialization register) by the 13-bit power frequency select word, PFS, allowing the power frequency to be defined in 8192 equal steps. The PFS word spans the two temporary registers R0 and R1.

The power frequency (\( f_{\text{power}} \)) is given by:
\[
f_{\text{power}} = \frac{f_{\text{Range}}}{8192} \times \text{PFS}
\]
where \( \text{PFS} \) = decimal value of the 13-bit PFS word and \( f_{\text{Range}} \) = power frequency range set in the initialization register.

#### Output inhibit selection
When active (i.e., low) the output inhibit bit INH sets all the PWM outputs to the off (low) state. No other internal operation of the device is affected. When the inhibit is released the PWM outputs continue immediately. Note that as the inhibit is asserted after the pulse deletion and pulse delay circuits, pulses shorter than the normal minimum pulse width may be produced initially.

#### Overmodulation selection
The overmodulation bit OM is, in effect, the ninth bit (MSB) of the amplitude word. When active (i.e., high) the output waveform will be controlled in the 100% to 200% range by the amplitude word.

The percentage amplitude control is now given by:
\[
\text{Overmodulated Amplitude} = \frac{A_{\text{power}}}{100}\%
\]
where \( A_{\text{power}} \) = the power amplitude

#### Amplitude selection
The power waveform amplitude is determined by scaling the amplitude of the waveform samples stored in the ROM by the value of the 8-bit amplitude select word (AMP).

The percentage amplitude control is given by:
\[
\text{Power Amplitude, } A_{\text{power}} = \frac{A}{255} \times 100\%
\]
where \( A \) = decimal value of AMP.

#### POWER-UP CONDITIONS
The Initialization register powerup with \( f_{\text{ARR}} \) 10kHz, \( f_{\text{Range}} \) 100 Hz, \( f_{\text{dy}} \) 2.5\( \mu \text{s} \), \( f_{\text{up}} \) 5\( \mu \text{s} \), and WS 0, and Control register powerup with zero. Holding RST low or using the SET TRIP input will ensure that the PWM outputs remain inactive (i.e., low) until the device is initialized.

#### COMMUNICATION COMMAND DESCRIPTION
This section defines the communication bytes sent and received by ETA2001.

The communication commands are described in Table 3.

### Acknowledgment
The device responds any recognized command received from microprocessor.

For the Writing/Setting commands, the response frame is one of follows:

- [ACK] [CHK] (2 bytes, indicates OK)
- [NAK] [CHK] (2 bytes, indicates ERROR)

For the Reading/Getting commands, if an ERROR occurs, the response frame is:

- [NAK] [CHK] (2 bytes, indicates ERROR)

Otherwise responds the corresponding DATA block.

#### Reading device version
The VER_RD command gets the device revision. The frame is 2 bytes:

- [VER_RD] [CHK]

And the device Response Packet:

- [VER_RD] [VER_SIZE] [...] […] [CHK]

The Response Packet size is VER_SIZE + 3 bytes.

#### Setting Baud rate
The default baud rate is always 9600 when power up. After power on, the baud rate can be set to a fast one. The value of baud rate is selected as shown in Table 4.

<table>
<thead>
<tr>
<th>BR_SEL</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
</tr>
</thead>
<tbody>
<tr>
<td>BR_VALUE</td>
<td>9600</td>
<td>14400</td>
<td>19200</td>
<td>28800</td>
<td>38400</td>
<td>57600</td>
<td>76800</td>
</tr>
</tbody>
</table>

### Table 4 Values of baud rate

The BR_WR command frame is 3 bytes:

- [BR_WR] [BR_SEL] [CHK]

#### Writing/Reading Initialization Register
The INIT_WR command frame is 7 bytes:

- [INIT_WR] [R0] [R1] [R2] [R3] [R4] [CHK]

The INIT_RD command frame is 2 bytes:

- [INIT_RD] [CHK]

And the device Response Packet is 7 bytes:

- [INIT_RD] [R0] [R1] [R2] [R3] [R4] [CHK]

#### Writing/Reading Control Register
The CTRL_WR command frame is 5 bytes:

- [CTRL_WR] [R0] [R1] [R2] [CHK]

The CTRL_RD command frame is 2 bytes:

- [CTRL_RD] [CHK]

And the device Response Packet is 5 bytes:

- [CTRL_RD] [R0] [R1] [R2] [CHK]

### ETA2001 PROGRAMMING EXAMPLE

#### Initialization Register Programming Example
A power waveform range of up to 250Hz is required with a carrier frequency of 6kHz, a pulse deletion time of 10\( \mu \text{s} \) and an underlap of 5\( \mu \text{s} \). The Sinusoid waveform is required.

1. Setting the carrier frequency
   - The carrier frequency should be set first as the power frequency, pulse deletion time and pulse delay time are all defined relative to the carrier frequency. We must calculate the value of cfs that will give the required carrier frequency:
The pulse width-registered in stored in the ROM. The power frequency range is shown in Table 1. Hence, temporary register R0 becomes in this case the value 00000000.

2. Setting the pulse delay time
We must calculate the value of \( \text{pdy} \) that will give the required pulse delay time:

\[
\text{pdy} = \text{t}_{\text{pd}} \times 2048
\]

\[
\text{pdy} = 5 \times 10^{-4} \times 6000.98 \times 2048 = 61.45
\]

However, the value of \( \text{pdy} \) must be an integer. As the purpose of the pulse delay is to prevent ‘shoot-through’ (where both top and bottom arms of the inverter are on simultaneously), it is sensible to round the pulse delay time up to a higher, rather than a lower figure.

Thus, if we assign the value 62 to \( \text{pdy} \) this gives a delay time of 5.05\( \mu \)s. \( \text{pdy} = 62 \) corresponds to a 8-bit PDY word of 00111110 in temporary register R2.

3. Setting the pulse deletion time
We must calculate the value of \( \text{pdt} \) that will give the required pulse deletion time:

\[
\text{pdt} = \text{t}_{\text{d}} \times 2048
\]

\[
\text{pdt} = 10 \times 10^{-5} \times 6000.98 \times 2048 = 122.90
\]

Again, \( \text{pdt} \) must be an integer and so must be either rounded up or down – the choice of which will depend on the application. Assuming we choose in this case the value 123 for \( \text{pdt} \), this gives a value of \( \text{pdt} \) of 10\( \mu \)s. \( \text{pdt} = 123 \) corresponds to a value of PDT, the 8-bit word in temporary register R3 of 01110110.

5. Setting waveform select
The Sinusoid waveform is selected by setting WS1 = 0 and WS2 = 0. Hence temporary register R4 should be set to 00000000.

6. Programming Initialization Register
The data in order to achieve the parameters in the example given, is shown in Table 5.

<table>
<thead>
<tr>
<th>Temporary Registers</th>
<th>R0</th>
<th>R1</th>
<th>R2</th>
<th>R3</th>
<th>R4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>CDH</td>
<td>84H</td>
<td>3EH</td>
<td>7BH</td>
<td>00H</td>
</tr>
</tbody>
</table>

Table 5 Initialization Data of example

The Writing Initialization Register command INIT_WR frame is shown in Table 6.

<table>
<thead>
<tr>
<th>Command</th>
<th>R0</th>
<th>R1</th>
<th>R2</th>
<th>R3</th>
<th>R4</th>
<th>CHK</th>
</tr>
</thead>
<tbody>
<tr>
<td>04H</td>
<td>CDH</td>
<td>84H</td>
<td>3EH</td>
<td>7BH</td>
<td>00H</td>
<td>0EH</td>
</tr>
</tbody>
</table>

Table 6 INIT_WR command frame of example

Control Register Programming Example
The control register would normally be updated many times while the motor is running, but just one example is given here. It is assumed that the initialization register has already been programmed with the parameters given in the previous example.

A power waveform of 100Hz is required with a PWM waveform amplitude of 80% of that stored in the ROM. The phase sequence should be set to give forward motor rotation. The outputs should be enabled and no overmodulation is required.

1. Setting the power frequency
The power frequency, \( f_{\text{POWER}} \), can be selected to 13-bit accuracy (i.e., 8192 equal steps) from 0Hz to \( f_{\text{RANGE}} \) as defined in the initialization register. In this case, \( f_{\text{RANGE}} = 250.04 \)Hz, the power frequency can be adjusted in increments of 0.03Hz.

\[
\text{f}_{\text{POWER}} = \frac{f_{\text{RANGE}}}{8192} \times \text{pfs}
\]

\[
\text{pfs} = 8192 \times \frac{f_{\text{RANGE}}}{250.04} = 3276.3
\]

We can only have \( \text{pfs} \) as an integer, so if we assign \( \text{pfs} = 3276 \) this gives \( f_{\text{POWER}} = 99.99 \)Hz. The 13-bit binary equivalent of this value gives a PFS word of 011001101100 in temporary registers R0 and R1.

2. Setting overmodulation, forward/reverse, output inhibit
Overmodulation is not required therefore OM = 0.
Forward motor control is required (i.e., the phase sequence of the PWM outputs should be red-yellow-blue) therefore forward/reverse bit F/R = 0.
Output inhibit should be inactive (i.e., the outputs should be active), therefore INH = 1.
These bits are all set in temporary register R1.

3. Setting the power waveform amplitude

\[
A_{\text{POWER}} = \frac{A}{255} \times 100\%
\]

\[
A = \frac{A_{\text{POWER}} \times 255}{100} = 80 \times 255 = 204
\]

The 8-bit binary equivalent of this value gives an AMP word of 01100110 in temporary register R2.

4. Programming Control Register
The data in order to achieve the parameters in the example given, is shown in Table 7.

<table>
<thead>
<tr>
<th>Temporary Registers</th>
<th>R0</th>
<th>R1</th>
<th>R2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>CCH</td>
<td>2CH</td>
<td>CCH</td>
</tr>
</tbody>
</table>

Table 7 Control Data of example

The Writing Control Register command CTRL_WR frame is shown in Table 8.

<table>
<thead>
<tr>
<th>Command</th>
<th>R0</th>
<th>R1</th>
<th>R2</th>
<th>CHK</th>
</tr>
</thead>
<tbody>
<tr>
<td>05H</td>
<td>CCH</td>
<td>2CH</td>
<td>CCH</td>
<td>CSH</td>
</tr>
</tbody>
</table>

Table 8 CTRL_WR command frame of example
In order to allow an external source to decouple an application of the power output, the PWM outputs are forced low (if not already low) thereby reducing noise sensitivity. The rising edge of ZPP corresponds to 0° for the output waveform.

Zero Phase Pulses (ZPP output)

The zero phase pulse output provides pulses at the same frequency as the power frequency. The rising edge of ZPP corresponds to 0° for the output waveform.

Low Power Crystal Oscillator

XTAL1 and XTAL2 are input and output, respectively, of an inverting amplifier which can be configured for use as an On-chip Oscillator, as shown in Fig. 13. A quartz crystal may be used. This Crystal Oscillator is a low power oscillator, with reduced voltage swing on the XTAL2 output. It gives the lowest power consumption, but is not capable of driving other clock inputs. The optimal value of the capacitors depends on the crystal or resonator in use, the amount of stray capacitance, and the electromagnetic noise of the environment. Some initial guidelines for choosing capacitors for use with crystals are given in Table 9.

![Crystal Oscillator Connections](image_url)

Fig. 13 Crystal Oscillator Connections

The Oscillator can operate in an optimized specific frequency range. The operating is selected as shown in Table 9.

<table>
<thead>
<tr>
<th>Frequency Range (MHz)</th>
<th>Capacitors C1 and C2 for Use with Crystals (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.0 - 16.0</td>
<td>12 - 22</td>
</tr>
</tbody>
</table>

Table 9 Crystal Oscillator Operating

APPLICATIONS INFORMATION

Circuit and Layout Considerations

The SET TRIP input forms a fast means of shutting down the inverter bridge by circumventing the latency associated with a microprocessor interrupt. It is recommended that the TRIP output is also linked to a microprocessor interrupt pin in order that the microprocessor is made aware of an incoming trip. It may then perform the necessary housekeeping following the inverter shut down. Although the SET TRIP input has a debounce circuit built in, the debounce period is necessarily short so that the speed with which the system may be shut down in an emergency is not compromised. It is therefore important to eliminate any possible source of noise from the SET TRIP input. It may be advantageous to place decoupling capacitors close to the SET TRIP pin if nuisance trips are of concern. The four PWM outputs each have a ±20mA drive capability enabling them to directly drive optocouplers for isolation purpose. Small transformers may also be driven directly, provided that due consideration is given to back emf generated at turn-off. In addition, the TRIP pin has a ±20mA drive capability to enable it to drive a status LED directly.

Fig. 14 shows a typical application of the ETA2001 to a single phase variable speed motor drive.
Fig. 14 A typical ETA2001 application
PACKAGE DETAILS
Dimensions are shown in: mm (in). For further package information, please contact your local Customer Service Centre.

24 - Lead Plastic Gull Wing Small outline Package (SOIC)