The ETA1001 PWM generator has been designed to provide waveforms for the grid tie inverters based on voltage-controlled mode with current harmonic compensation, control of variable speed AC machines, uninterruptible power supplies and other forms of power electronic devices which require pulse width modulation as a means of efficient power control.

The four TTL level PWM outputs (Fig. 2) control the four switches in a single-phase inverter bridge. This is usually via an external isolation and amplification stage.

The ETA1001 is fabricated in CMOS for low power consumption.

Information contained within the pulse width modulated sequences controls the shape, power frequency, and amplitude of the output waveform. Parameters such as the carrier frequency, minimum pulse width, pulse delay time and phaser offset may be defined during the initialization of the device. The pulse delay time (underlap) controls the delay between turning on and off the two power switches in each output leg of the inverter bridge, in order to accommodate variations in the turn-on and turn-off times of families of power devices.

The ETA1001 is easily controlled by a microprocessor or PC and its fully-digital generation of PWM waveforms gives unprecedented accuracy and temperature stability. Precision pulse shaping capability allows optimum efficiency with any power circuitry. The device operates as a stand-alone microprocessor peripheral, reading the power waveform directly from an internal ROM and requiring microprocessor intervention only when operating parameters need to be changed. Alternatively, the ETA1001 can work independently with the operating parameters stored in the internal E²PROM.

A Universal Asynchronous serial Receiver and Transmitter (UART) is used to receive/transmit data from/to the microprocessor/controller.

Rotational frequency is defined to 13 bits for high accuracy and a zero setting is included in order to implement DC injection braking with no software overhead.

The standard pure sinusoid wave shape is available to cover most applications. In addition, any symmetrical wave shape can be integrated on-chip to order.

FEATURES
- Fully Digital Operation
- UART Interfaces
- Power-Frequency Range up to 2kHz
- 13-Bit Speed Control Resolution
- Carrier Frequency Selectable up to 25kHz
- Waveform Stored in Internal ROM
- Double Edged Regular Sampling
- Selectable Minimum Pulse Width and Underlap Time
- Phaser Offset Selectable up to ±30°
- Selectable Operating Mode
- Grid-Tie Anti-Islanding Resolution
- Auto Grid-Tie Phase Sequence Synchronization
- Current Harmonic Compensation
- DC Injection Braking

APPLICATIONS
- Grid-Tie Inverters
- Single Phase Induction Motor Speed Controllers
- Uninterruptible Power Supplies
- Static Inverter Power Supplies
- Power Waveform Generators

ORDERING INFORMATION
- ETA1001: 24-lead SOIC, industrial temp range.
ETA1001

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):

\[ V_{CC} = +5V \pm 5\% , \ T_{AMB} = +25^\circ C \]

**DC Characteristics**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Value (Min.)</th>
<th>Value (Typ.)</th>
<th>Value (Max.)</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input high voltage</td>
<td>( V_{IH} )</td>
<td>2.7</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Input low voltage</td>
<td>( V_{IL} )</td>
<td>1.1</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Input leakage current</td>
<td>( I_{IN} )</td>
<td>1</td>
<td></td>
<td>( \mu A )</td>
<td>( V_{IN} = GND ) or ( V_{CC} )</td>
</tr>
<tr>
<td>Output high voltage</td>
<td>( V_{OH} )</td>
<td>4.2</td>
<td></td>
<td></td>
<td>V ( I_{OH} = -20 \ mA )</td>
</tr>
<tr>
<td>Output low voltage</td>
<td>( V_{OL} )</td>
<td>0.7</td>
<td></td>
<td></td>
<td>V ( I_{OL} = 20 \ mA )</td>
</tr>
<tr>
<td>Supply current (static)</td>
<td>( I_{CC} ) (static)</td>
<td>5.5</td>
<td>10</td>
<td>24</td>
<td>mA Idle 16 MHz</td>
</tr>
<tr>
<td>Supply current (dynamic)</td>
<td>( I_{CC} ) (dynamic)</td>
<td>14</td>
<td>24</td>
<td></td>
<td>mA Active 16 MHz</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>( V_{CC} )</td>
<td>4.5</td>
<td>5.0</td>
<td>5.5</td>
<td>V</td>
</tr>
</tbody>
</table>

**AC Characteristics**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Value (Min.)</th>
<th>Value (Typ.)</th>
<th>Value (Max.)</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock frequency</td>
<td>( f_{CLK} )</td>
<td>8</td>
<td>16</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Clock duty cycle</td>
<td>( D_{CLK} )</td>
<td>40</td>
<td>60</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>SET TRIP = 1 ( \rightarrow ) outputs tripped ( \rightarrow TRIP = 0 )</td>
<td>( t_{TRIP} )</td>
<td>0.25</td>
<td>25</td>
<td>( \mu S )</td>
<td></td>
</tr>
</tbody>
</table>

**ABSOLUTE MAXIMUM RATINGS**

Supply voltage, \( V_{CC} \) .............. .............. .............. 6.0V
Voltage on any pin .............. .............. 1.0V to \( V_{CC} +0.5V \)
Current through any I/O pin .......... .............. 20.0 mA
Storage temperature .............. .............. -65°C to +150°C
Operating temperature range ....... .............. -40°C to +105°C

Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**PIN DESCRIPTIONS**

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Name</th>
<th>Type</th>
<th>Function</th>
<th>Pin No.</th>
<th>Name</th>
<th>Type</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>LT</td>
<td>O</td>
<td>Left-side, Top power switch</td>
<td>24</td>
<td>LB</td>
<td>O</td>
<td>Left-side, Bottom power switch</td>
</tr>
<tr>
<td>2</td>
<td>OS</td>
<td>O</td>
<td>Output Status; low = no output</td>
<td>23</td>
<td>GSYNC</td>
<td>I</td>
<td>Grid SYNC pulse</td>
</tr>
<tr>
<td>3</td>
<td>TRIP</td>
<td>O</td>
<td>Output trip status; active low</td>
<td>22</td>
<td>VG</td>
<td>I</td>
<td>Voltage of Grid</td>
</tr>
<tr>
<td>4</td>
<td>SET TRIP</td>
<td>I</td>
<td>Set output trip</td>
<td>21</td>
<td>OMS2</td>
<td>I</td>
<td>Operating Mode Selection bit-2</td>
</tr>
<tr>
<td>5</td>
<td>TXD</td>
<td>O</td>
<td>UART TX</td>
<td>20</td>
<td>OMS1</td>
<td>I</td>
<td>Operating Mode Selection bit-1</td>
</tr>
<tr>
<td>6</td>
<td>VCC</td>
<td>P</td>
<td>Positive power supply</td>
<td>19</td>
<td>DCAP</td>
<td>P</td>
<td>Decoupling CAPacitor</td>
</tr>
<tr>
<td>7</td>
<td>GND</td>
<td>P</td>
<td>Negative power supply (0V)</td>
<td>18</td>
<td>GND</td>
<td>P</td>
<td>Negative power supply (0V)</td>
</tr>
<tr>
<td>8</td>
<td>RT</td>
<td>O</td>
<td>Right-side, Top power switch</td>
<td>17</td>
<td>VCC</td>
<td>P</td>
<td>Positive power supply</td>
</tr>
<tr>
<td>9</td>
<td>RB</td>
<td>O</td>
<td>Right-side, Bottom power switch</td>
<td>16</td>
<td>OMS0</td>
<td>I</td>
<td>Operating Mode Selection bit-0</td>
</tr>
<tr>
<td>10</td>
<td>XTL1</td>
<td>I</td>
<td>XTL Input</td>
<td>15</td>
<td>RST</td>
<td>I</td>
<td>Reset internal counters, active low</td>
</tr>
<tr>
<td>11</td>
<td>XTL2</td>
<td>O</td>
<td>XTL Output</td>
<td>14</td>
<td>GSYNC</td>
<td>I</td>
<td>Grid SYNC pulse</td>
</tr>
<tr>
<td>12</td>
<td>RXD</td>
<td>I</td>
<td>UART RX</td>
<td>13</td>
<td>NC</td>
<td>-</td>
<td>Not Connect</td>
</tr>
</tbody>
</table>
FUNCTIONAL DESCRIPTION

An asynchronous method of PWM generation is used with uniform or 'double-edged' regular sampling of the waveform stored in the internal ROM as illustrated in Fig. 3.

The triangle carrier wave frequency is selectable up to 25kHz, enabling ultrasonic operation for noise critical applications. Power frequency ranges of up to 2kHz are possible, with the actual output frequency resolved to 13-bit accuracy within the chosen range in order to give precise motor speed control and smooth frequency changing. The output phase sequence of the PWM outputs can also be changed to allow both forward and reverse motor operation.

PWM output pulses can be 'tailored' to the inverter characteristics by defining the minimum allowable pulse width (the ETA1001 will delete all shorter pulses from the 'pure' PWM pulse train) and the pulse delay (underlap) time, without the need for external circuitry. This gives cost advantages in both component savings and in allowing the same PWM circuitry to be used for control of a number of different inverter drive circuits simply by changing the microprocessor software.

The grid–tie phaser offset is selectable up to ±30° per 0.234° step, enabling compensation for phase sync pulse delay.

The motor braking can be implemented by setting the rotational speed to 0Hz. This is termed 'DC injection braking', in which the rotation of the motor is opposed by allowing DC to flow in the windings.

A trip input allows the PWM outputs to be shut down immediately, overriding the microprocessor control in the event of an emergency.

Other possible ETA1001 applications are as a 1-phase waveform generator as part of a switched-mode power supply (SMPS) or of an uninterruptible power supply (UPS). In such applications the high carrier frequency allows a very small switching transformer to be used.

MICROPROCESSOR INTERFACE

The ETA1001 interfaces to the controlling microprocessor by means of a standard UART.

Byte Format

- Baud Rate: The baud rate can be set to one of follows: 9600, 14400, 19200, 28800, 38400, 57600 and 76800, the device is always set to 9600 baud rate when power on.
- Serial Bit Format: 1 Start Bit, 8 Data Bits, 1 Stop Bit
- + 10 Bits Total

Block Format

A Communication Block is defined as a Command byte, optional data bytes, and a CHK byte. A block is limited to a maximum of sixteen (16) bytes.

- CHK Byte: A CHK byte must be sent at the end of each block of data. The CHK byte is a checksum calculated by adding the Command byte and all DATA bytes. The CHK byte is not included in the summation. The carry bit for CHK additions is ignored since the CHK byte is limited to eight bits.

The following example shows a CHK byte calculation for a CTRL_WR command sent to the device. See COMMUNICATION COMMAND DESCRIPTION for details of byte meanings.

05H WRITE Control Register
B8H R0
27H R1
FFH R2
+ -----------------------------
1E3H Therefore the CHK byte would be equal to E3H

A checksum will be performed on all full blocks of communication.
The ETA1001 can be configured as grid-tie or stand-alone Single-Phase PWM Waveform Generator by Operating Mode Selection bits OMS2...0.

The Operating Modes are determined as shown in Table 1.

<table>
<thead>
<tr>
<th>Mode</th>
<th>OMS2</th>
<th>OMS1</th>
<th>OMS0</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Stand-alone, the power frequency ($f_{\text{POWER}}$) 50Hz(^{(1)})</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Stand-alone, the power frequency ($f_{\text{POWER}}$) 60Hz(^{(1)})</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Stand-alone, set via UART</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Stand-alone, output with current status(^{(1)})</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Grid-tie, the power frequency ($f_{\text{POWER}}$) 50Hz(^{(1)})</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Grid-tie, the power frequency ($f_{\text{POWER}}$) 60Hz(^{(1)})</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Grid-tie, set the power frequency ($f_{\text{POWER}}$) via UART</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Grid-tie, the power frequency ($f_{\text{POWER}}$) auto detected(^{(1)})</td>
</tr>
</tbody>
</table>

Note: 1. Writing control data via the UART will ignore $f_{\text{POWER}}$.

### CONTROLLING THE ETA1001

The ETA1001 is controlled by loading data into a 48-bit initialization register and a 24-bit control register via the UART interface.

The initialization register would normally be loaded before motor operation (i.e., prior to the PWM outputs being activated) and sets up the basic operating parameters associated with the inverter and motor. The control register is used to control the PWM outputs during operation e.g., stop/start, speed, amplitude etc. and would normally be loaded and changed only after the initialization register has been loaded.

### Initialization Register Function

The 48-bit initialization register contains parameters which, under normal operation, will be defined during the power-up sequence. These parameters can be stored into the internal EPROM in advance, and will be loaded into the initialization register automatically on power-up. Changing these parameters during a PWM cycle is valid, regardless the PWM outputs are inhibited (low) or active.

The parameters set in the initialization register are as follows:

#### Carrier frequency

Low carrier frequencies reduce switching losses where as high carrier frequencies increase waveform resolution and can allow ultrasonic operation.

#### Power frequency range

This sets the maximum power frequency that can be carried within the PWM output waveforms. This would normally be set to a value to prevent the motor system being operated outside its design parameters.

#### Pulse delay time (‘underlap’)

For each phase of the PWM cycle there are two control signals, one for the top switch connected to the positive inverter DC supply and one for the bottom switch connected to the negative inverter DC supply. In theory, the states of these two switches are always complementary. However, due to the finite and non-equal turn-on and turn-off times of power devices, it is desirable when changing the state of the output pair, to provide a short delay time during which both outputs are off in order to avoid a short circuit through the switching elements.

#### Pulse deletion time

A pure PWM sequence produces pulses which can vary in width between 0% and 100% of the duty cycle. Therefore, in theory, pulse...
widths can become infinitesimally narrow. In practice this causes problems in the power switches due to storage effects and therefore a minimum pulse width time is required. All pulses shorter than the minimum specified are deleted.

**Waveform**

The power waveform is included as standard with the ETA1001: Sinusoid.

**Voltage of Grid**

The grid-tie inverter based on voltage-controlled mode has an advantage of power supplying to common customers directly without stand-alone and grid-tie mode-transition problems compared with that in current-controlled mode. For reducing output current distortion, the ETA1001 has an algorithm of current harmonic compensation according to the voltage of Grid side. The voltage is not indispensable but it is beneficial to reduce the total harmonic distortion.

**Phaser Offset**

This compensates the offset of grid-tie phase sync pulse.

**Initialization Register Programming**

The initialization register data is loaded in 8-bit segments into the six 8-bit temporary registers R0-R5. When all the initialization data has been loaded into these registers it is transferred into the 48-bit initialization register.

```
<table>
<thead>
<tr>
<th>CFS2</th>
<th>CFS1</th>
<th>CFS0</th>
</tr>
</thead>
</table>
```

**ARRIER FREQUENCY SELECT WORD BITS 0-7**

CFS2 = LSB

**Fig. 4 Temporary register R0**

```
<table>
<thead>
<tr>
<th>FRS2</th>
<th>FRS1</th>
<th>FRS0</th>
<th>CFS12</th>
<th>CFS11</th>
<th>CFS10</th>
<th>CFS9</th>
</tr>
</thead>
</table>
```

**FREQUENCY RANGE SELECT WORD BITS 8-12**

CFS12 = MSB

**Fig. 5 Temporary register R1**

**Carrier frequency selection**

The carrier frequency is selected as a proportion of the preconcerted frequency by the 13-bit carrier frequency select word, CFS.

The carrier frequency, \( f_{\text{CARR}} \), is then given by:

\[
 f_{\text{CARR}} = \frac{1 \times 10^4 \times cfs}{2048}
\]

where \( 25 \leq cfs \leq 5120 \). If CFS selected out of the range, it will be limited to the boundary.

**Power frequency range selection**

The power frequency range selected here defines the maximum limit of the power frequency. The operating power frequency is controlled by the 13-bit Power Frequency Select (PFS) word in the control register but may not exceed the value set here.

The power frequency range is a function of the carrier waveform frequency \( f_{\text{CARR}} \) and a multiplication factor \( m \), determined by the 3-bit FRS word. The value of \( m \) is determined as shown in Table 2.

<table>
<thead>
<tr>
<th>FRS word</th>
<th>101</th>
<th>100</th>
<th>011</th>
<th>010</th>
<th>001</th>
<th>000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value of ( m )</td>
<td>32</td>
<td>16</td>
<td>8</td>
<td>4</td>
<td>2</td>
<td>1</td>
</tr>
</tbody>
</table>

**Table 2 Values of carrier frequency multiplication factor \( m \)**

The power frequency range, \( f_{\text{RANGE}} \), is then given by:

\[
 f_{\text{RANGE}} = \frac{f_{\text{CARR}}}{384} \times m
\]

where \( f_{\text{CARR}} = \) carrier frequency and \( m = 1, 2, 4, 8, 16 \) or 32 (as set by FRS).

**Pulse delay time**

The pulse delay time affects all four PWM outputs by delaying the rising edges of each of the outputs by an equal amount.

The pulse delay time is a function of the carrier waveform frequency and \( pdy \), defined by the 8-bit pulse delay time select word (PDY).

The pulse delay time, \( t_{\text{pdy}} \), is then given by:

\[
 t_{\text{pdy}} = \frac{pdy \times f_{\text{CARR}}}{2048}
\]

where \( pdy = 0 - 255 \) (as set by PDY) and \( f_{\text{CARR}} = \) carrier frequency.

**Pulse deletion time**

To eliminate short pulses the true PWM pulse train is passed through a pulse deletion circuit. The pulse deletion circuit compares pulse widths with the pulse deletion time set in the initialization register. If a pulse (either positive or negative) is greater than or equal in duration to the pulse deletion time, it is passed through unaltered, otherwise the pulse is deleted.

The pulse deletion time, \( t_{\text{pdy}} \), is a function of the carrier waveform frequency and \( pdt \), defined by the 8-bit pulse deletion time word (PDT).

The pulse deletion time, \( t_{\text{pdt}} \), is then given by:

\[
 t_{\text{pdt}} = \frac{pdt \times f_{\text{CARR}}}{2048}
\]

where \( pdt = 0 - 255 \) (as set by PDT) and \( f_{\text{CARR}} = \) carrier frequency.

**Waveform Selection**

The waveform is included as standard with the ETA1001. The pure sine wave is available for applications where waveform purity is important such as static inverter power supplies, uninterruptible power supplies and for driving single or to phase induction motors.

**Fig. 6 Temporary register R2**

**Fig. 7 Temporary register R3**

**Fig. 8 Temporary register R4**

Two bits, WS0 and WS1, are used to define the power waveform, according to Table 3:

<table>
<thead>
<tr>
<th>Value</th>
<th>Waveform</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>Sinusoid (default)</td>
</tr>
<tr>
<td>0 1</td>
<td>Reserved</td>
</tr>
<tr>
<td>1 0</td>
<td>Reserved</td>
</tr>
<tr>
<td>1 1</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

**Table 3 Waveform selection**

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Voltage of Grid
If the voltage of grid is available, set VG bit to one, otherwise clear the bit. It allows the harmonics in the grid voltage to be injected into the waveform.

<table>
<thead>
<tr>
<th>PHO</th>
<th>PHO</th>
<th>PHO</th>
<th>PHO</th>
<th>PHO</th>
<th>PHO</th>
<th>PHO</th>
<th>PHO</th>
</tr>
</thead>
<tbody>
<tr>
<td>PHASER OFFSET</td>
<td>SELECT WORD</td>
<td>PHO = LSB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Fig. 9 Temporary register R5

Phaser Offset
The offset is a signed value from -127 to 127. A negative value lags the phase and a positive value leads the phase.
The offset phase angle ($\phi_{offset}$) is given by:

$$\phi_{offset} = \frac{90}{384} \times \text{pho}$$

where pho = -127 - 127 (as set by PHO)

Control Register Function
This 24-bit register contains the parameters that would normally be modified during PWM cycles in order to control the operation of the inverter.
The parameters set in the control register are as follows:

Power frequency (speed)
Allows the power frequency of the PWM outputs to be adjusted within the range specified in the initialization register

Power frequency amplitude
By altering the widths of the PWM output pulses while maintaining their relative widths, the amplitude of the power waveform is effectively altered whilst maintaining the same power frequency.

Output inhibit
Allows the outputs to be set to the low state while the PWM generation continues internally. Useful for temporarily inhibiting the outputs without having to change other register contents.

Control Register Programming
The control register should only be programmed once the initialization register contains the basic operating parameters of the ETA1001.

As with the initialization register, control register data is loaded into the three 8-bit temporary registers R0 - R2. When all the data has been loaded into these registers it is transferred into the 24-bit control register.

Power frequency selection
The power frequency is selected as a proportion of the power frequency range (defined in the initialization register) by the 13-bit power frequency select word, PFS, allowing the power frequency to be defined in 8192 equal steps. The PFS word spans the two temporary registers R0 and R1.
The power frequency ($f_{\text{power}}$) is given by:

$$f_{\text{power}} = \frac{\text{f}_{\text{range}} \times \text{pfs}}{8192}$$

where pfs = decimal value of the 13-bit PFS word and f_{range} = power frequency range set in the initialization register.

In modes 0, 1, 3, 4, 5 and 7, $f_{\text{power}}$ is read only. All writing $f_{\text{power}}$ operation will be ignored.

Output inhibit selection
When active (i.e., low) the output inhibit bit INH sets all the PWM outputs to the off (low) state. No other internal operation of the device is affected. When the inhibit is released the PWM outputs continue immediately. Note that as the inhibit is asserted after the pulse deletion and pulse delay circuits, pulses shorter than the normal minimum pulse width may be produced initially.

<table>
<thead>
<tr>
<th>AMP</th>
<th>AMP</th>
<th>AMP</th>
<th>AMP</th>
<th>AMP</th>
<th>AMP</th>
<th>AMP</th>
<th>AMP</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMPLITUDE SELECT WORD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AMP = LSB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Fig. 12 Temporary register R2

Amplitude selection
The power waveform amplitude is determined by scaling the amplitude of the waveform samples stored in the ROM by the value of the 8-bit amplitude select word (AMP).
The percentage amplitude control is given by:

$$\text{Power Amplitude, A}_{\text{power}} = \frac{A}{255} \times 100\%$$

where A = decimal value of AMP.

POWER-UP CONDITIONS
The Initialization register power-up with $f_{\text{AMP}}$ 20kHz, $f_{\text{range}}$ 100 Hz, $t_{\phi_2}$ 2.5μs, $t_{\phi_1}$ 5μs, VG 0 and $\phi_{offset}$ 0, and Control register power-up with zero.

In modes 0, 1, 4, 5 and 7, the Control register PFS is initialized automatically according to Table 1 Function.

In modes 2 and 6, the Control register should be initialized via UART. Holding RST low or using the SET TRIP input will ensure that the PWM outputs remain inactive (i.e., low) until the device is initialized.

COMMUNICATION COMMAND DESCRIPTION
This section defines the communication bytes sent and received by ETA1001.

<table>
<thead>
<tr>
<th>Command</th>
<th>Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACK</td>
<td>00H</td>
<td>Response Code, OK</td>
</tr>
<tr>
<td>NAK</td>
<td>FFH</td>
<td>Response Code, ERROR</td>
</tr>
<tr>
<td>VER_RD</td>
<td>81H</td>
<td>Read device version</td>
</tr>
<tr>
<td>BR_WR</td>
<td>02H</td>
<td>Set Baud rate</td>
</tr>
<tr>
<td>INIT_WR</td>
<td>04H</td>
<td>Write Initialization Register</td>
</tr>
<tr>
<td>INIT_RD</td>
<td>84H</td>
<td>Read Initialization Register</td>
</tr>
<tr>
<td>CTRL_WR</td>
<td>05H</td>
<td>Write Control Register</td>
</tr>
<tr>
<td>CTRL_RD</td>
<td>85H</td>
<td>Read Control Register</td>
</tr>
<tr>
<td>REG_STA</td>
<td>06H</td>
<td>Store Initialization Register and Control Register to E(^{\text{PROM}})</td>
</tr>
<tr>
<td>REG_DEL</td>
<td>86H</td>
<td>Delete Initialization Register and Control Register from E(^{\text{PROM}})</td>
</tr>
</tbody>
</table>

Table 4 UART Command
Acknowledgment

The device responds any recognized command received from microprocessor.

For the Writing/Setting commands, the response frame is one of follows:

[ACK] [CHK] (2 bytes, indicates OK)
[NAK] [CHK] (2 bytes, indicates ERROR)

For the Reading/Getting commands, if an ERROR occurs, the response frame is:

[NAK] [CHK] (2 bytes, indicates ERROR)
Otherwise responds the corresponding DATA block.

Reading device version

The VER_RD command gets the device revision. The frame is 2 bytes:

[VER_RD] [CHK]
And the device Response Packet:

[VER_RD] [VER_SIZE] [...] [CHK]
The Response Packet size is VER_SIZE + 3 bytes.

Setting Baud rate

The default baud rate is always 9600 when power up. After power on, the baud rate can be set to a fast one. The value of baud rate is selected as shown in Table 5.

<table>
<thead>
<tr>
<th>BR_SEL</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
</tr>
</thead>
<tbody>
<tr>
<td>BR_VALUE</td>
<td>9600</td>
<td>14400</td>
<td>19200</td>
<td>28800</td>
<td>38400</td>
<td>57600</td>
<td>76800</td>
</tr>
</tbody>
</table>

The carrier frequency should be set first as the power frequency, sinusoid 10kHz, a pulse deletion time of 5μs and an underlap of 2.5μs. The Sinusoid waveform is required, the voltage of grid is available and no phaser offset.

1. Setting the carrier frequency

The carrier frequency should be set first as the power frequency, pulse deletion time and pulse delay time are all defined relative to the carrier frequency. We must calculate the value of cfs that will give the required carrier frequency:

\[ f_{carr} = \frac{1 \times 10^6}{2048} \times \text{cfs} \]

\[ \text{cfs} = \frac{2048 \times f_{carr}}{1 \times 10^6} = \frac{2048 \times 1 \times 10^4}{1 \times 10^6} = 2048 \]

The 13-bit binary equivalent of this value gives a CFS word of 010000000000 in temporary registers R0 and R1.

2. Setting the power frequency range

We must calculate the value of m that will give the required power frequency:

\[ f_{range} = \frac{f_{carr}}{384} \times m \]

\[ m = \frac{384 \times f_{range}}{f_{carr}} = \frac{384 \times 100}{1 \times 10^4} = 3.84 \]

From Table 2, we assign m = 4 corresponds to a 3-bit FRS word of 010 in temporary register R1. This gives \( f_{range} = 104.17 \) Hz.

3. Setting the pulse delay time

As the pulse delay time affects the actual minimum pulse width seen at the PWM outputs.

We must calculate the value of pdy that will give the required pulse delay time:

\[ t_{pd} = \frac{f_{carr} \times 2048}{f_{pdy}} \]

\[ f_{pdy} = \frac{f_{carr} \times 2048}{2.5 \times 10^4} = 2048 = 51.2 \]

However, the value of pdy must be an integer. As the purpose of the pulse delay is to prevent ‘shoot-through’ (where both top and bottom arms of the inverter are on simultaneously), it is sensible to round the pulse delay time up to a higher, rather than a lower figure.

Thus, if we assign the value 52 to pdy this gives a delay time of 5.54μs. pdy = 52 corresponds to a 8-bit PDY word of 00110100 in temporary register R2.

4. Setting the pulse deletion time

We must calculate the value of pdt that will give the required pulse deletion time:

\[ t_{pdt} = \frac{f_{carr} \times 2048}{f_{pdt}} \]

\[ f_{pdt} = \frac{f_{carr} \times 2048}{5 \times 10^4} = 2048 = 102.4 \]

Again, pdt must be an integer and so must be either rounded up or down – the choice of which will depend on the application. Assuming we choose in this case the value 103 for pdt, this gives a value of tpd of 5.03μs. pdt = 103 corresponds to a value of PDT, the 8-bit word in temporary register R3 of 01100111.

5. Setting waveform select

The Sinusoid waveform is only one to be selected, the WS word should be set to 00 in temporary register R4.

6. Setting voltage of grid status

The voltage of grid is available, thus the bit VG should be set to 1 in temporary register R4.

7. Setting phaser offset

No phaser offset required, set temporary register R5 to 0.

8. Programming Initialization Register

The data in order to achieve the parameters in the example given, is shown in Table 6.

<table>
<thead>
<tr>
<th>Temporary Registers</th>
<th>R0</th>
<th>R1</th>
<th>R2</th>
<th>R3</th>
<th>R4</th>
<th>R5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>00H</td>
<td>48H</td>
<td>34H</td>
<td>67H</td>
<td>08H</td>
<td>00H</td>
</tr>
</tbody>
</table>

Table 6 Initialization Data of example

The Writing Initialization Register command INIT_WR frame is shown in Table 7.
Control Register Programming Example

The control register would normally be updated many times while the inverter is working, but just one example is given here. It is assumed that the initialization register has already been programmed with the parameters given in the previous example.

The mode 7 (Grid-tie, the power frequency \( f_{\text{power}} \) auto detected) is required with a PWM waveform amplitude of 80% of that stored in the ROM.

1. Setting the power frequency

The power frequency, \( f_{\text{power}} \), can be selected to 13-bit accuracy (i.e. 8192 equal steps) from 0Hz to \( f_{\text{range}} \) as defined in the initialization register. In this case, \( f_{\text{power}} \) is auto detected, we assign \( pfs = 0 \) or ignore it. The 13-bit binary equivalent of this value gives a PFS word of 0000000000000 or xxxxxxxxxxxx in temporary registers R0 and R1.

2. Setting output inhibit

Output inhibit should be inactive (i.e., the outputs should be active), therefore \( \text{INH} = 1 \).

These bits are all set in temporary register R1.

3. Setting the power waveform amplitude

\[
A_{\text{power}} = \frac{A}{255} \times 100\%
\]

\[
A = \frac{A_{\text{power}} \times 255}{100} = \frac{80 \times 255}{100} = 204
\]

The 8-bit binary equivalent of this value gives an AMP word of 11001100 in temporary register R2.

4. Programming Control Register

The data in order to achieve the parameters in the example given, is shown in Table 8.

<table>
<thead>
<tr>
<th>Temporary Registers</th>
<th>R0</th>
<th>R1</th>
<th>R2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>00H</td>
<td>20H</td>
<td>CCH</td>
</tr>
</tbody>
</table>

Table 8 Control Data of example

The Writing Control Register command CTRL_WR frame is shown in Table 9.

<table>
<thead>
<tr>
<th>Command</th>
<th>R0</th>
<th>R1</th>
<th>R2</th>
<th>CHK</th>
</tr>
</thead>
<tbody>
<tr>
<td>05H</td>
<td>00H</td>
<td>00H</td>
<td>00H</td>
<td>ECH</td>
</tr>
</tbody>
</table>

Table 9 CTRL_WR command frame of example

The typical ETA1001 programming routine is shown in Fig 13.

HARDWARE INPUT/OUTPUT FUNCTIONS

Set Output Trip (SET TRIP input)

The SET TRIP input is provided separately from the microprocessor interface in order to allow an external source to override the microprocessor and provide a rapid shutdown facility. For example, logic signals from over current sensing circuitry or the microprocessor 'watchdog' might be used to activate this input.

When the SET TRIP input is taken to logic high, the output trip latch is activated. This results in the TRIP output and the four PWM outputs being latched low immediately. This condition can only be cleared by applying a reset cycle to the RST input. It is essential that when not in use SET TRIP is tied low and isolated from potential sources of noise; on no account should it be left floating.

SET TRIP is latched internally at the master clock rate in order to reduce noise sensitivity.

Output Trip Status (TRIP output)

The TRIP output indicates the status of the output trip latch and is active low.

Reset (RST input)

The RST input performs the following functions when active (low):

1. All PWM outputs are forced low (if not already low) thereby turning off the drive switches.

2. All internal counters are reset to zero (this corresponds to 0° for the waveform output).

3. The rising edge of RST reactivates the PWM outputs resetting the output trip and setting the TRIP output high – assuming that the SET TRIP input is inactive (i.e. low).

Output Status (OS output)

The OS output indicates the status of the PWM outputs and active high. If the PWM outputs stopped (Reset, Output trip or Output inhibit), the OS output low.

Grid Sync pulse (two GSYNC input)

The two grid sync pulse inputs are used for grid-tie modes only. They are required 50% (±10%) duty cycle.

Voltage of Grid (VG input)

The analog signal VG is used for injecting harmonic into the pure sinusoid waveform. The signal should limit to 0 to 5V.

Operating Mode Selection (OMS2..0 input)

The OMSn inputs configure the operating mode. For details see Table 1.

Low Power Crystal Oscillator

XTAL1 and XTAL2 are input and output, respectively, of an inverting amplifier which can be configured for use as an On-chip Oscillator, as shown in Fig. 14. A quartz crystal may be used.

This Crystal Oscillator is a low power oscillator, with reduced voltage swing on the XTAL2 output. It gives the lowest power consumption, but is not capable of driving other clock inputs.

C1 and C2 should always be equal for both crystals and resonators. The optimal value of the capacitors depends on the crystal or resonator in use, the amount of stray capacitance, and the electromagnetic noise of the environment. Some initial guidelines for choosing capacitors for use with crystals are given in Table 10.
The Oscillator can operate in an optimized specific frequency range. The operating is selected as shown in Table 10.

<table>
<thead>
<tr>
<th>Frequency Range (MHz)</th>
<th>Capacitors C1 and C2 for Use with Crystals (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.0 - 16.0</td>
<td>12 - 22</td>
</tr>
</tbody>
</table>

**Table 10 Crystal Oscillator Operating**

**APPLICATIONS INFORMATION**

**Grid-Tie Anti-Islanding Resolution**

In mode 7, ETA1001 performs grid-tie anti-islanding auto control. In this case, ETA1001 detects the grid power frequency and outputs PWM waveform with a -3% frequency offset. When the grid cut off, the output frequency decrease continuously until it trigger anti-islanding event to stop PWM output. ETA1001 will auto restart PWM output after grid restoration.

**Circuit and Layout Considerations**

The SET TRIP input forms a fast means of shutting down the inverter bridge by circumventing the latency associated with a microprocessor interrupt. It is recommended that the TRIP output is also linked to a microprocessor interrupt pin in order that the microprocessor is made aware of an incoming trip. It may then perform the necessary housekeeping following the inverter shut down.

Although the SET TRIP input has a debounce circuit built in, the debounce period is necessarily short so that the speed with which the system may be shut down in an emergency is not compromised. It is therefore important to eliminate any possible source of noise from the SET TRIP input. It may be advantageous to place decoupling capacitors close to the SET TRIP pin if nuisance trips are of concern.

In the same way, the two GSYNC inputs should also be cautious to deal with the noise.

The four PWM outputs each have a ±20mA drive capability, enabling them to directly drive optocouplers for isolation purpose. Small transformers may also be driven directly, provided that due consideration is given to back emf generated at turn-off. In addition, the TRIP pin has a ±20mA drive capability to enable it to drive a status LED directly.

Fig. 15 and Fig 16 show most typical applications of the ETA1001 to single phase inverter.
Grid-tie Single Phase Inverter with Mode 7 (power frequency auto detect)
Grid-Tie Island Auto Control
Grid-tie and Stand-alone Switching Enable

Fig. 15 Grid-tie single phase inverter
Fig. 16 Single phase variable speed motor drive
PACKAGE DETAILS
Dimensions are shown in: mm (in). For further package information, please contact your local Customer Service Centre.

**WARNING:** DO NOT USE IN LIFE SUPPORT EQUIPMENT. ETA semiconductor products are not authorized for use as critical components in life support devices or systems without the express written approval.